Shallow Trench Isolation Chemical Mechanical Planarization: Slurry chemistry, Cleaning chemistry, and Mechanisms

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Abstract

The increasing adoption of emerging technologies such as autonomous driving, artificial intelligence, 5G communications, the Internet of Things, and large-scale data processing has created a need for a robust and dependable semiconductor industry worldwide. In order to meet this demand, new device architectures have been introduced, including FinFETs, 3D-stacked technology, gate-all-around nanosheet, complementary field-effect transistor devices, and others. These cutting-edge architectures rely heavily on chemical mechanical planarization (CMP) and post-CMP cleaning processes, which are essential enabling technologies.

This presentation will describe the development of CMP slurries and post-CMP cleaning solutions through a fundamental understanding of various chemical and mechanical phenomena such as slurry chemistry, interfacial force measurement, surface adsorption, and surface characterization/ modification occurring at the wafer interface during shallow trench isolation (STI) CMP. Normally, ceria-based slurries are employed in STI CMP due to their ability to provide high, tunable, and self-stopping removal rates for several dielectric films. We demonstrated that the synthesis methods significantly influence the surface chemistry of ceria abrasives, which impacts their overall efficiency in the removal rates of the SiO_2 surface. Size-dependent surface chemistry of ceria particles and their interactions with the SiO_2 surface during polishing was also investigated. However, ceria particles are prone to creating defects, and their complete removal from the substrate after polishing is also challenging. Recently, we reported cleaning solutions to rupture a strong chemical bonding between ceria particles and the SiO_2 films via a nucleophilic attack that could almost completely remove even 10 nm-sized ceria particles from SiO_2 surfaces during cleaning.